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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,246	12/10/2003	Seok-Kyu Lee	053933-5059	5700
9629	7590	02/26/2007	EXAMINER	
MORGAN LEWIS & BOCKIUS LLP 1111 PENNSYLVANIA AVENUE NW WASHINGTON, DC 20004			PATEL, ISHWARBHAI B	
ART UNIT		PAPER NUMBER		
2841				
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	02/26/2007	PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/731,246	LEE ET AL.
	Examiner Ishwar (I. B.) Patel	Art Unit 2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 27 November 2006.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-25 is/are pending in the application.  
 4a) Of the above claim(s) 1-16 and 23-25 is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 17-20 and 22 is/are rejected.  
 7) Claim(s) 21 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 10 December 2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 6, 2006 has been entered.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusagaya (US Patent Application Publication Number 2003/0063453) in view of Kuwako (US Patent No. 6,693,793) and Steigerwald (US Patent No. 5,912,809).

**Regarding claim 17**, Kusagaya in figure 7, discloses a printed circuit board with embedded capacitors, comprising: an inner layer of a multi-layered printed circuit board having a copper clad laminate adhered thereon by means of an adhesive (L4, as shown in detail in figure 1, described at paragraph 0071 in detail); a ground layer copper foil

(L2, shown in detail in figure 1), formed at a top and a bottom of the -inner layer; a polymer capacitor paste (polymer film 16) having a predetermined thickness formed on the ground layer copper foil, a power layer (L3, as shown in detail in figure 1) copper foil formed on the capacitor paste (16) and partitioned (see figure), an insulation layer attached copper film (48) formed on the power layer copper foil (14 and 48, figure 5); a blind via-hole (18) and a through-hole (20) formed at predetermined portions of the insulation layer-attached copper film; and plated layers of the blind via-hole and the through-hole for layer connection of the printed circuit board.

Kusagaya does not disclose the ground layer copper foil with roughened surface and the polymer film made of capacitor paste having high dielectric constant and the power layer copper foil are divided into cells corresponding to each operation voltage.

Kuwako, in figure 1, discloses a doubled sided copper clad laminate for capacitor layer formation with roughened (14) surface for better adhesion, column 5, line 35-50.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Kusagaya with the ground layer copper foil with roughened surface, as taught by Kuwako, in order to have better adhesion.

Regarding the polymer film made of paste having high dielectric constant. Kusagaya discloses the polymer film (16) provided between the ground layer and power layer made of polyimide film, but is silent about the dielectric constant of the polymer film. However, Kusagaya further states that the combination of ground layer, polymer layer and power layer, is used as a condenser body, page 2, paragraph 0028. It is

known (scientifically) in the art that the capacity (capacitance) of the condenser will depend upon the dielectric constant of the polymer (insulation) between the conductive layers (power and ground layers). Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Kusagaya with the polymer layer between the ground layer and the power layer formed of high dielectric constant, in order to have the desired capacitor (condenser) capacity.

Regarding the limitation "a dry film pattern that is laminated on the power layer copper foil and is etched by use of an etching mask," it is a process limitation in a product claim. Such a process limitation defines the claimed invention over the prior art to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is same as, or obvious over the prior art. See Product-by-Process in MPEP § 2113 and 2173.05(p) and *In re Thorpe*, 777 F.2d 695, 227 USPQ 964, 966 (Fed. Cir. 1985). Kusagaya discloses the structure. Therefore, Kusagaya meets the limitations.

Regarding the limitation, the power layer copper foil are divided into cells corresponding to each operation voltage, though, Kusagaya shows the power layer patterned as required, see figure 7, does not explicitly recites the same is divided into cell corresponding to each operation volatage. However, power layer divided into areas of different potential for respective components is old and known in the art. Steigerwald

in figure 3 discloses a printed circuit board with the power layer segmented to provide various power supply voltage for different component (column 5, line 53-62).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to further modify the Structure of Kusagaya with the power layer copper foil divided into cells corresponding to each operation voltage, as taught by Steigerwald, in order to have various capacitive plane for different components.

**Regarding claim 18**, the modified circuit board of Kusagaya further discloses the insulation layer-attached copper film is a resin-coated copper foil (14-48, figure 6).

**Regarding claim 19**, the modified circuit board of Kusagaya further discloses the surface of the ground layer copper foil is roughened at a thickness of 1-2  $\mu\text{m}$  to increase a bonding force between the ground layer copper foil and the capacitor paste (Kuwako, claim 4).

4. Claims 20 and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over the modified circuit board of Kusagaya as applied to claim 17 above, and further in view of Bruno (US Patent No. 5,155,072).

**Regarding claim 20**, the combination of Kusagaya, Kuwako and Steigerwald discloses all the features of the claimed invention as applied to claim 17 above, but does not disclose the capacitor mixture is in a mixed composite form of  $\text{BaTiO}_3$  ceramic powders having high-dielectric constant of 1000-10,000 and polyimide.

Bruno discloses a high dielectric composition having BaTiO<sub>3</sub> with a dielectric constant of at least 10,000 for electric device such as capacitors. Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified circuit board of Kusagaya with the capacitor paste in a mixed composite form of BaTiO<sub>3</sub> ceramic powders having high-dielectric constant of 1000-10,000 and polyimide, as taught by Bruno, in order to have the desired capacitance value.

**Regarding claim 22**, the modified circuit board of Kusagaya discloses all the features of the claimed invention as applied to claim 17 above, but does not disclose the capacitor paste is coated at a thickness of 8-25  $\mu\text{m}$ . However, it is scientifically known in the art that the capacitance of a capacitor will depend upon the dielectric constant and the thickness of the insulating layer between the two conductive layer and the desired value can be obtain by a specific combination of the dielectric constant and thickness of the insulating layer. Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified circuit board of Kusagaya with

the capacitor paste coated with a thickness of 8-25  $\mu\text{m}$ , in order to have desired capacitance value.

***Allowable Subject Matter***

5. Claim 21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

6. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tran (US Patent No. 5,764,491) in figure 2 discloses a circuit board with the power plane divided into cells for respective component to be mounted on the component layer.

Rethlingshoefer et al. (Japanese Patent No. JP41013005A) discloses a high dielectric paste made with resin.

Toshiharu et al. (Japanese Patent No. JP02001267751A) discloses a capacitor incorporating substrate with dielectric film formed on the roughened surface of copper foil.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ibp  
February 16, 2007

  
Ishwar (I. B.) Patel  
Primary Examiner